Bihar Engineering University, Patna
End Semester Examination - 2022

Course: B.Tech.
Code: 101302

Semester: III
Subject: Basic Electronics

Time: 03 Hours
Full Marks: 70

Instructions:-
(i) The marks are indicated in the right-hand margin.
(ii) There are **NINE** questions in this paper.
(iii) Attempt **FIVE** questions in all.
(iv) Question No. 1 is compulsory.

Q.1 **Choose the correct option of the following:(Answer any seven)** [2 x 7 = 14]

(a) In a semiconductor diode, the barrier potential offers
 (i) Opposition to free electrons in the N region and holes in P region
 (ii) Opposition to minority carriers in P region and majority carriers in N region
 (iii) Opposition to only minority carriers in both regions
 (iv) Opposition to only majority carriers in both regions

(b) A diode is a
 (i) Non-linear device
 (ii) Bilateral device
 (iii) Linear device
 (iv) None of the above

(c) The emitter of transistor is
 (i) Lightly doped
 (ii) Heavily doped
 (iii) Moderately doped
 (iv) None of the above

(d) A transistor is a _____ operated device.
 (i) Current
 (ii) Voltage
 (iii) Both voltage and current
 (iv) None of the above

(e) For I_{DSS} =9mA, V_P= -3.5V and V_{GS} = -2V, value of I_D is
 (i) 9 mA   (ii) 1.65 mA   (iii) 2.55 mA   (iv) 10 mA

(f) Which of the following statement is true about FET?
 (i) It has high output impedance
 (ii) It has high input impedance
 (iii) It has low input impedance
 (iv) It does not offer any resistance

(g) For a JFET, the value of V_{DS} at which I_D becomes essentially constant is the
 (i) Pinch-off voltage
 (ii) Cut-off voltage
 (iii) Breakdown voltage
 (iv) Ohmic voltage

(h) Slew rate is defined as the:
 (i) Maximum rate of change of output voltage with time
 (ii) Minimum rate of change of output voltage with time
 (iii) Moderate rate of change of output voltage with time
 (iv) None of the above

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(i) In a BJT if the both emitter and collector junction are reverse biased it is said
(i) active
(ii) saturation
✓(iii) cut off
(iv) none of above

(j) A differential amplifier has a differential gain of 20000, CMRR = 80dB. The common mode gain is given by
(i) 2   (ii) 1   (iii) ½   (iv) 0

Q.2 (a) Discuss with the help of circuit diagram, the purpose of providing negative feedback and positive feedback.   [7]

(b) Draw the circuit diagram of voltage-shunt feedback amplifier and derive the expression of closed-loop voltage gain using op-amp.   [7]

Q.3 (a) Explain the working of BJT as an amplifier.   [7]

(b) With a neat circuit diagram explain the Voltage Divider Bias circuit by giving its exact analysis.   [7]

Q.4 (a) Explain op-amp as Differentiator and Integrator. Also draw the output Waveforms of the same.   [7]

(b) Calculate the CMMR (in decibel) for the circuit measurement of V_d = 1 MV, V_o=120MV, V_c=1mV and V_o=20µV.   [7]

Q.5 (a) Describe the RC Phase-shift oscillator with circuit diagram.   [7]

(b) A single-stage amplifier has voltage gain of 10 and bandwidth of 1MHZ. Three such stage are cascaded and negative feedback of 10% is applied to the cascade stage. Find out the overall voltage gain and bandwidth of cascade stage with feedback.   [7]

Q.6 (a) Write the properties of ideal operational amplifier.   [7]

(b) Draw the pin configuration of 741 op-amp IC. Explain its working.   [7]

Q.7 (a) Draw basic structure of n-channel JFET and describe its working operation.   [7]

(b) Draw transfer curve. Also, Explain briefly the construction and working of p-channel enhancement MOSFET.   [7]

Q.8 (a) Draw circuit diagram of transistor amplifier in CE, CB, CC configuration. Discuss the comparison of their important characteristics.   [7]

(b) Discuss the need for stabilization? List the various factors responsible for shift in Q-point in a transistor. Explain the effect of each parameter on stability of Q-point.   [7]

Q.9 Write short notes on any two of the following: [7x2]
(i) UJT
(ii) SCR
(iii) Zener diode
(iv) Photo diode